Claims

What is claimed is:

[c1] A computer chip comprising a power supply, comprising:

chip logic; and

a clock tree that comprises at least one clock driver, wherein power distributed from the power supply to the clock tree is isolated from power distributed from the power supply to the chip logic.

[c2] The computer chip of claim 1, further comprising:

a capacitor, wherein power distributed from the power supply to the capacitor is isolated from power distributed from the power supply to the chip logic.

[c3] The computer chip of claim 1, wherein the chip logic comprises at least one logic element.

[c4] The computer chip of claim 1, wherein the clock tree comprises at least one clock driver.

[c5] The computer chip of claim 1, further comprising:

a first lead through a circuit board to the computer chip, wherein the first lead is used to distribute power from the power supply to the clock tree; and

a second lead through the circuit board to the computer chip, wherein the second lead is used to distribute power from the power supply to the chip logic.

[c6] The computer chip of claim 5, wherein the first lead runs through a chip package, and wherein the second lead runs through the chip package.

[c7] A method for reducing clock skew, comprising:

drawing current from a power supply for chip logic operations; and

drawing current from the power supply for clock tree operations,

wherein the current drawn from the power supply for the chip logic operations is isolated from the current drawn from the power supply for the clock tree operations.

[c8] The method of claim 7, wherein the clock tree comprises a clock generator and at least one clock driver.

[c9] The method of claim 7, wherein the chip logic comprises at least one logic element.

[c10] The method of claim 7, further comprising:

drawing current from the power supply to decouple noise, wherein the current drawn from the power supply to decouple noise is isolated from the current drawn for the chip logic operations.

[c11] The method of claim 7, further comprising:

using separate leads through a chip package to distribute power from the power supply to the clock tree and the chip logic.

[c12] The method of claim 7, further comprising:

using separate leads through a circuit board to distribute power from the power supply to the clock tree and the chip logic.